

Fig. 1
(Prior Art)

Title: MEMORY CIRCUIT SCAN ARRANGEMENT

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Docket No. 851963.401

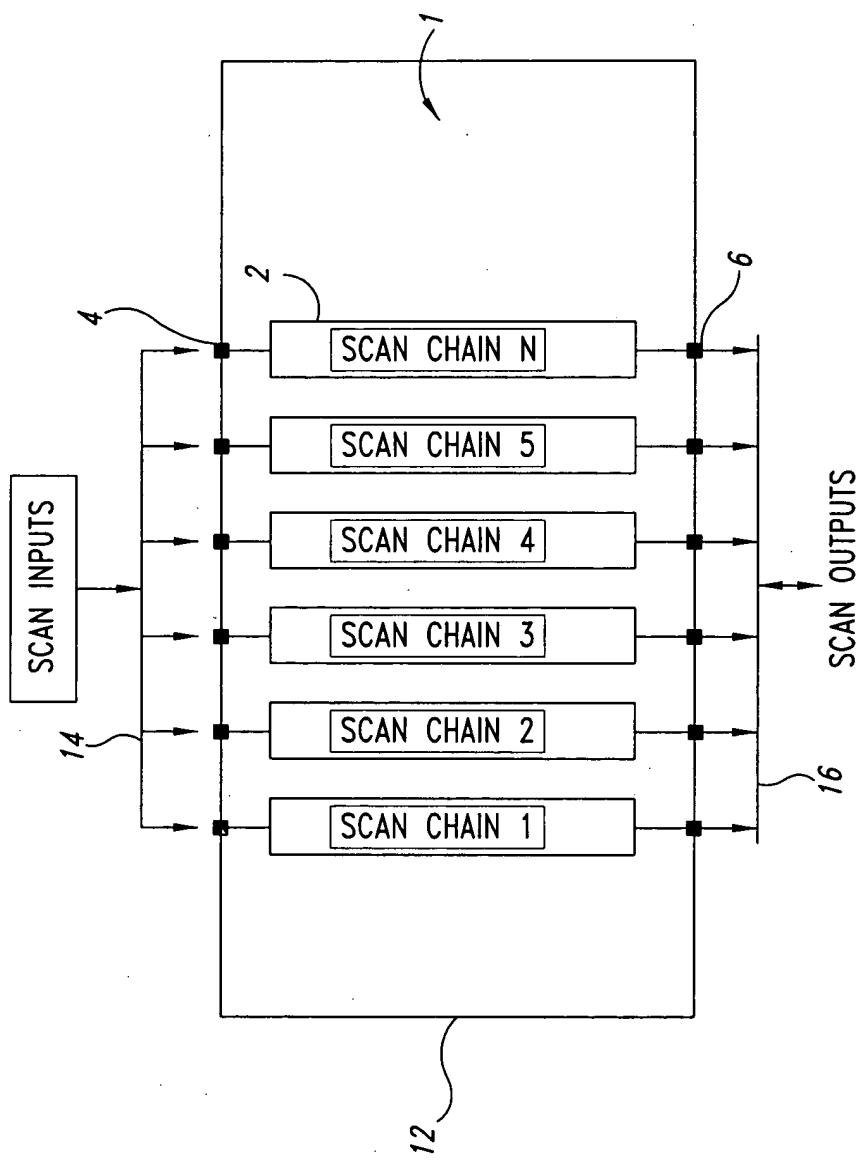


Fig. 2
(Prior Art)

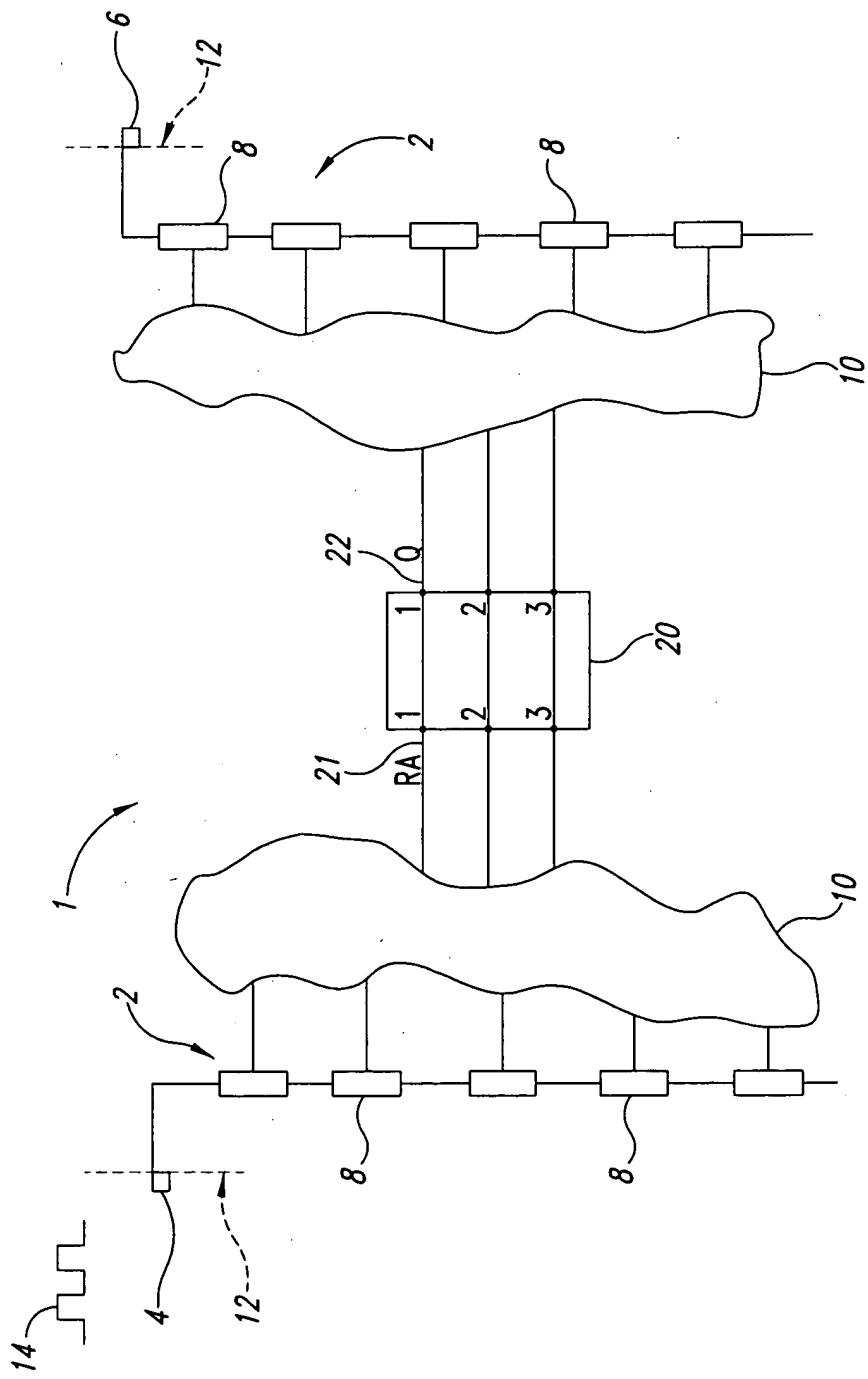


Fig. 3
(Prior Art)

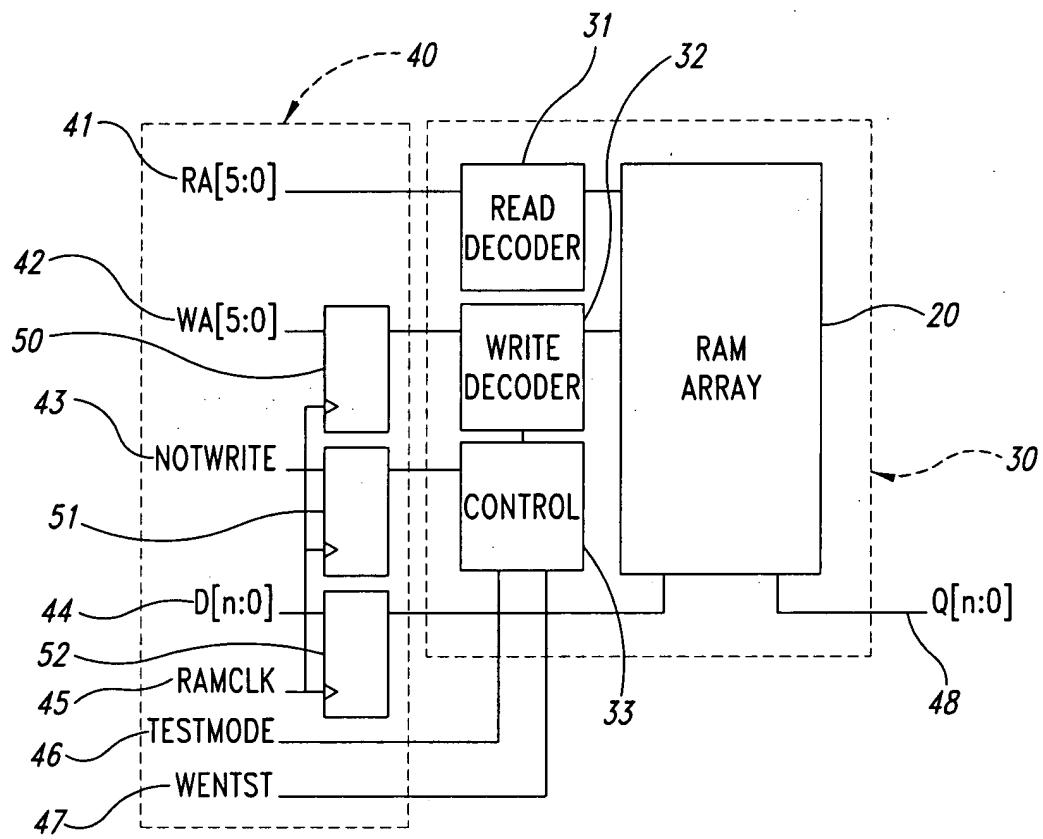


Fig. 4

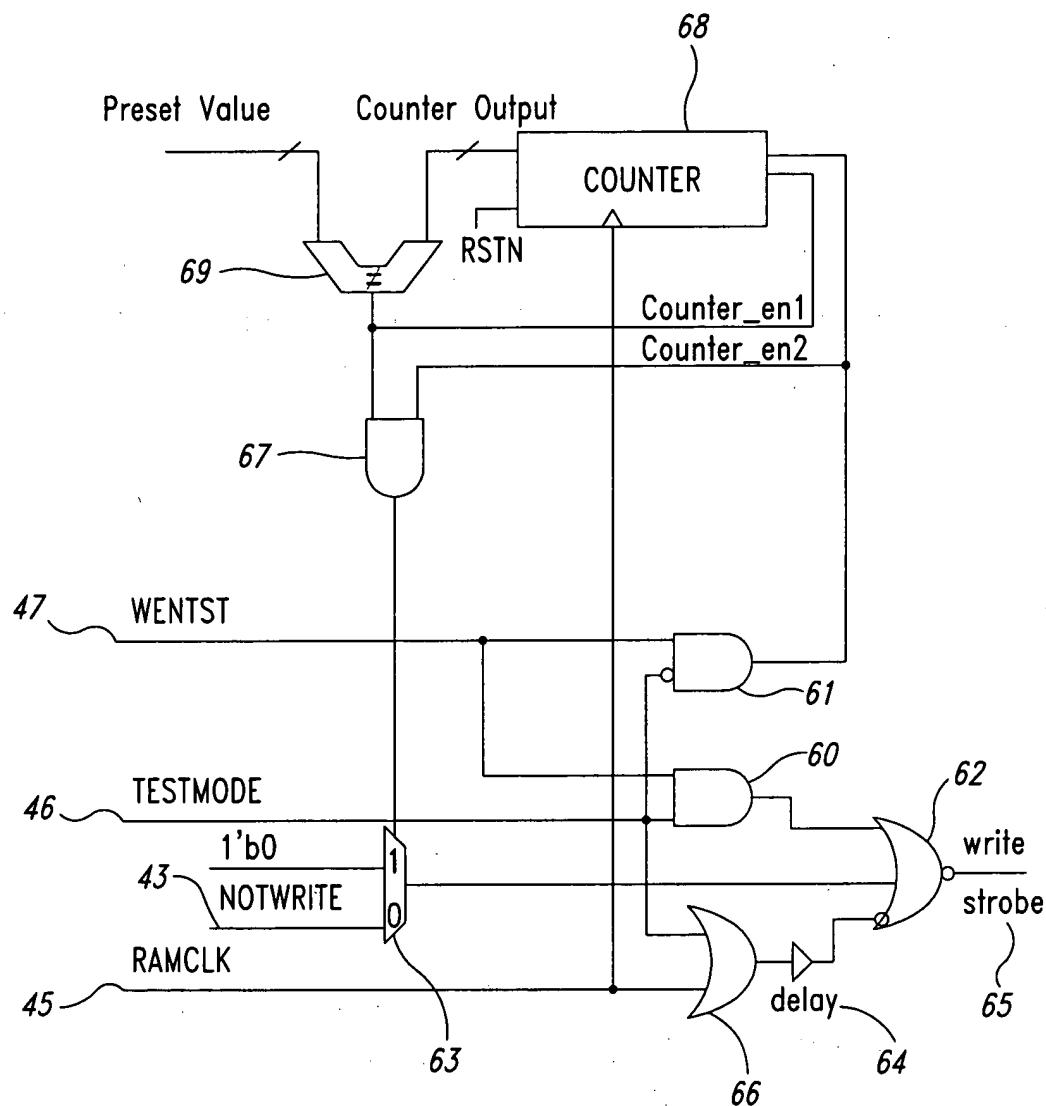


Fig. 5

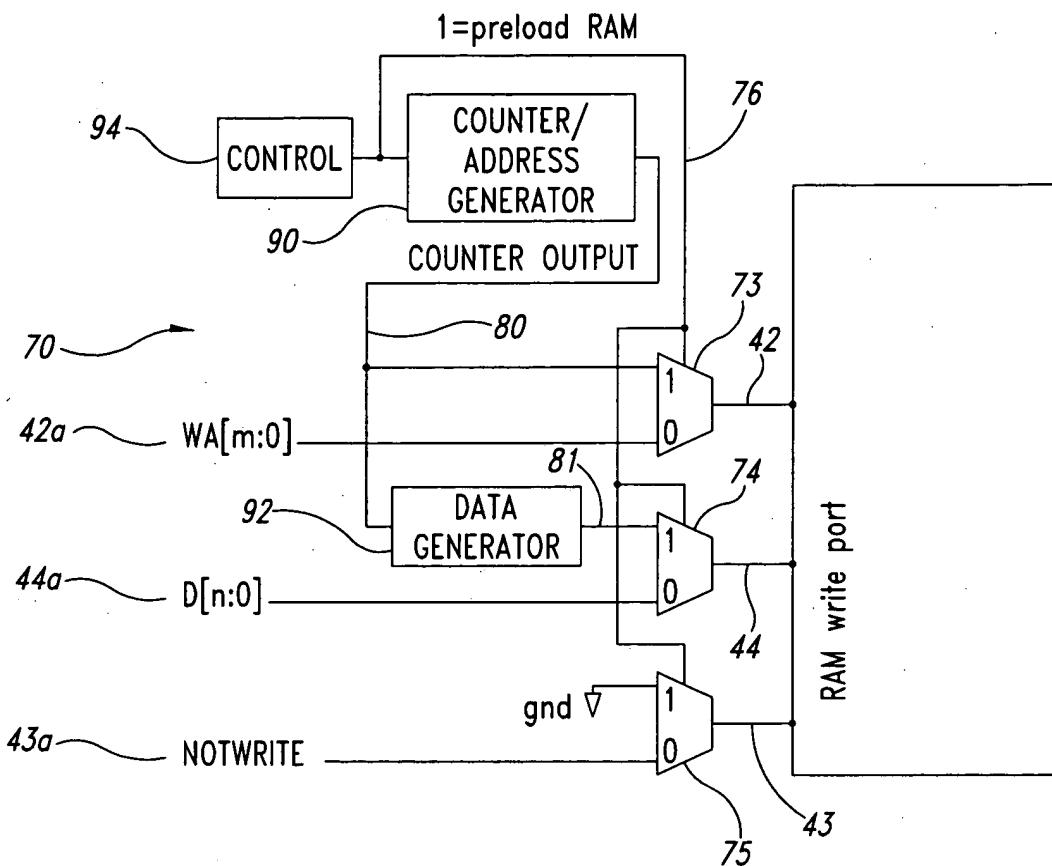


Fig. 6

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address=001	0	1	0	0	1	0	0	1
address=010	1	0	0	1	0	0	1	0
address=011	1	1	0	1	1	0	1	1
address=100	0	0	1	0	0	1	0	0
address=101	0	1	1	0	1	1	0	1
address=110	1	0	1	1	0	1	1	0
address=111	1	1	1	1	1	1	1	1

data bit 7

data bit 6

data bit 5

data bit 4

data bit 3

data bit 2

data bit 1

data bit 0

Fig. 7

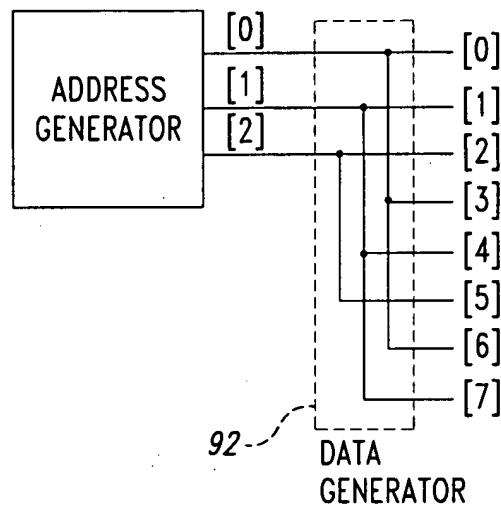


Fig. 8

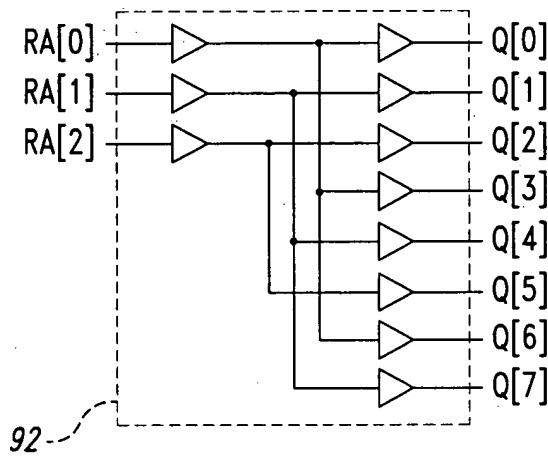


Fig. 9

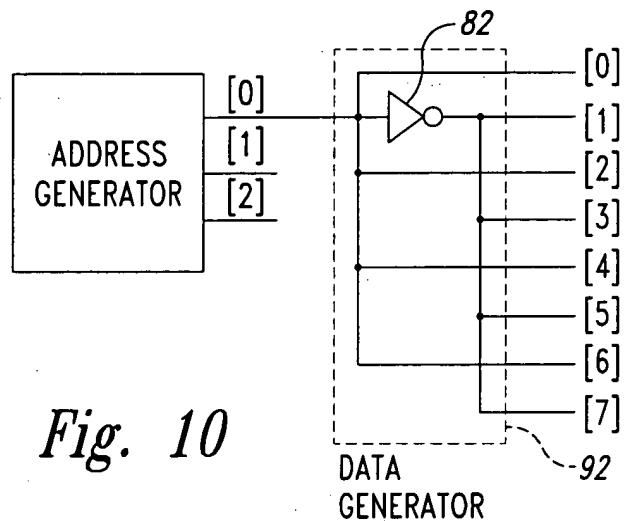


Fig. 10

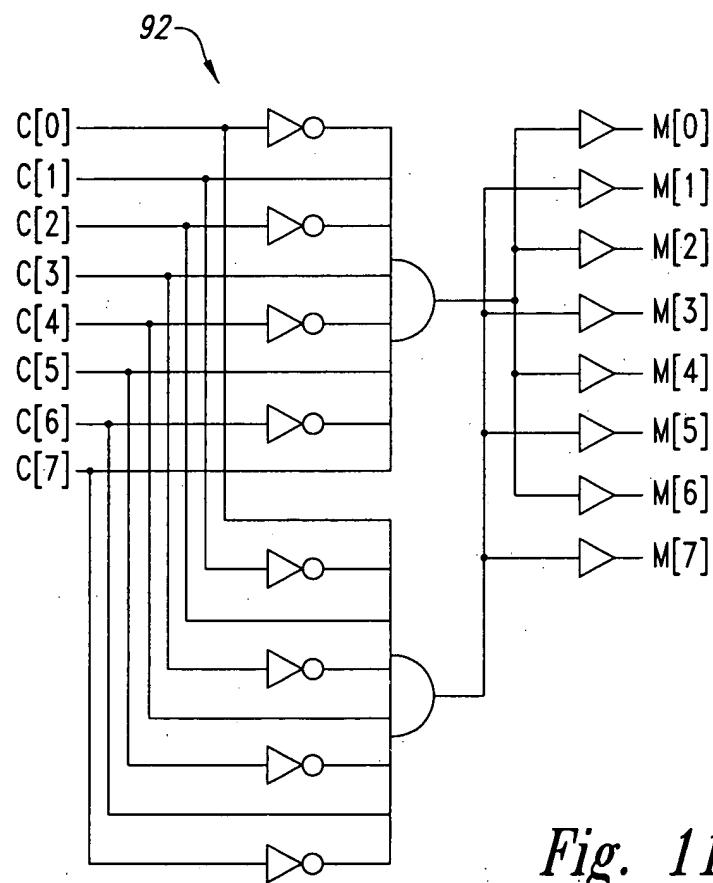


Fig. 11

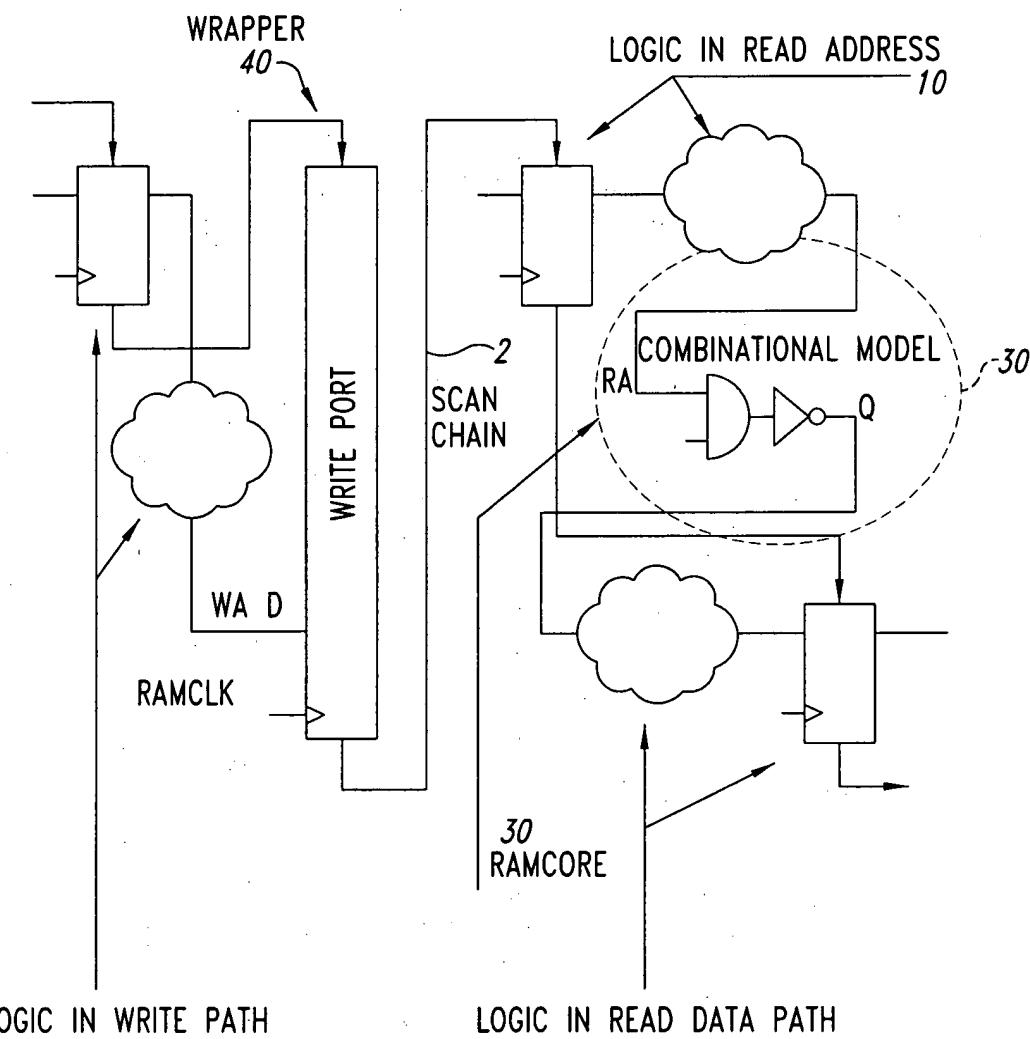


Fig. 12